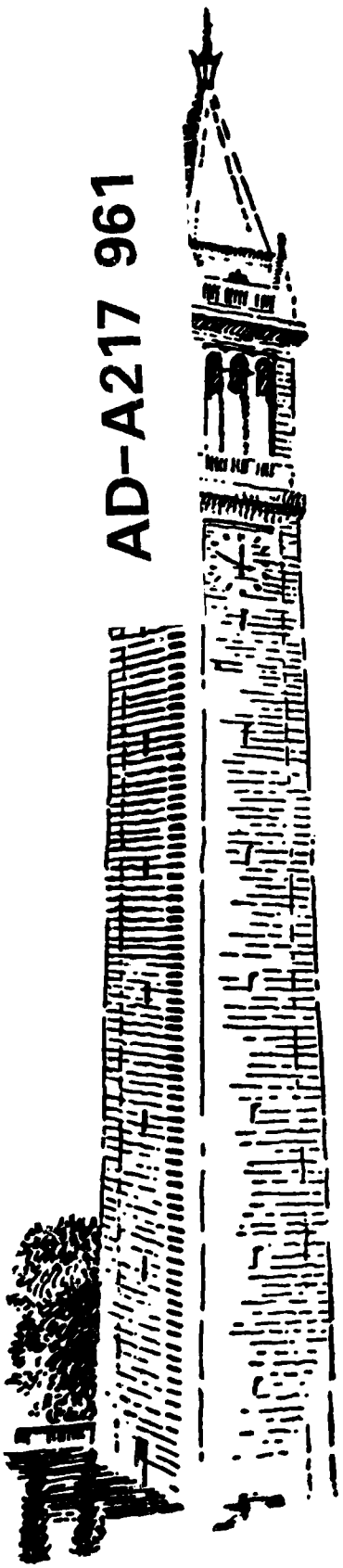

Report No. UCB/ERL 89/1

JOINT SERVICES ELECTRONICS PROGRAM

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W. G. Oldham

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This document is the 1989 annual report of research conducted in the Electronics Research Laboratory at University of California at Berkeley under the sponsorship of the Joint Services Electronics Program. The research is organized under two theme areas: High-speed wide-band elements for high-frequency electronics and new architectures for parallel computation. The former has 5 work units and one supplement ranging from optoelectronic, Gunn-effect, ultra-short-channel Si and superconductive devices to new techniques for electromagnetic scattering computation. The second theme area has 3 work units which cover research projects ranging from CAD techniques for the synthesis of very large circuits and investigations of alternative architectures for parallel computation to devices for use in neural networks. One project is concerned with biologically-based neural networks.

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PART A - DIRECTOR'S OVERVIEW

This JSEP Program is organized into two theme areas: high-speed wide-band elements for high-frequency electronics and new architectures for parallel computation. The former has 5 work units and one supplement ranging from optoelectronic, Gunn-effect, ultra-short-channel Si and superconductive devices to new techniques for electromagnetic scattering computation. The second theme area has 3 work units which cover research projects ranging from CAD techniques for the synthesis of very large circuits and investigations of alternative architectures for parallel computation to devices for use in neural networks. One project is concerned with biologically-based neural networks. Numerous publications, presentations and papers have resulted, and we include in the next section four descriptions of especially significant accomplishments: 1) the discovery of hot electron effects in devices which occur at voltages less than the bandgap potential, 2) new designs for Gunn-effect oscillators which have unprecedented power and efficiency, 3) achievement of three unique guided wave devices, and 4) a technique to achieve fault tolerance in artificial neural networks.

The JSEP program continues to be a vital component of the research program of the Electronics Research Laboratory. Of some 74 faculty in the laboratory, 12 are partially supported by JSEP. Some 30 students received JSEP support during 1989, and 4 M.S. and Ph.D. theses were produced.

The enclosed Annual Report Appendix includes copies of 19 published articles, 10 papers submitted to journals, 5 conference papers, and 4 theses. In some cases only abstracts are included.

PART B - SIGNIFICANT ACCOMPLISHMENTS

Low-Voltage Hot-Electron Effects in Deep-Submicrometer MOSFETs

J. Chung, M.-C. Jeng, J.E. Moon, P.K. Ko, and C. Hu

Because of hot-electron reliability limitations, the power supply voltage for future VLSI systems will have to be reduced. It has been hoped that for drain biases lower that some critical value (e.g. 2.7V), electrons would not be able to gain sufficient energy to generate gate current or to cause interface damage and device degradation regardless of the amount that the channel length is reduced.

The deep-submicrometer MOSFETs used in this study [1] were fabricated using an NMOS technology for which the deep-submicrometer gates were obtained by calibrated thinning of the optically defined photoresist patterns in oxygen plasma, a technique developed under the JSEP program.[2] Figs. 2 and 3 display substrate and gate current as a function of drain voltage for different channel lengths. For the L_{eff} = 0.1μm device, I_{Sub} is observed at V_{Drain} = 0.7V; I_{Gate} is observed at V_{Drain} = 1.75V. In Fig. 3, the percent change in the charge-pump current is plotted as a function of time for different stress voltages. No change in the time dependence is observed for stress voltages as low as 1.8V. A slope of $n \approx 0.5$ is observed which is in agreement with previously reported values for both I-V and charge-pump degradation.

It is evident that substrate current is present at drain voltages well below what is considered the threshold energy for impact ionization (≈1.65eV) as well as the silicon bandgap energy at room temperature (1.1eV). It is also evident that gate current is present at drain voltages well below the Si-SiO_2 barrier height, even including the effects of barrier lowering (≈2.7eV). The critical energy for interface trap generation is reported to be 3.7eV. A simple lucky-electron model, in which carriers gain all their kinetic energy from the applied external potential, is not adequate to explain this low-voltage behavior.

The mechanism for electrons to obtain high energies is not identified yet. It may be electron-electron scattering, duger recombination, or electron phonon interaction.

Publications

[1] J. Chung, M.C. Jeng, J.E. Moon, P.K. Ko, and C. Hu, "Low-Voltage Hot Electron Degradation in Deep Submicrometer MOSFETs," *International Reliability Physics Symposium Proceedings*, Phoenix, AZ, April 1989, pp. 92-97.

[2] J. Chung, M.C. Jeng, J.E. Moon, A.T. Wu, T.Y. Chan, P.K. Ko, and C. Hu, "Deep Submicron MOS Device Fabrication Using a Photoresist- Ashing Technique," *IEEE Electron Device Letters*, Vol. EDL-9, No. 4, April 1988, pp. 186-188.

[3] J. Tang and K. Hess, "Theory of Hot Electron Emission from Silicon into Silicon Dioxide," *J. Appl. Phys.*, Vol. 54, p. 5145, Sep. 1983.

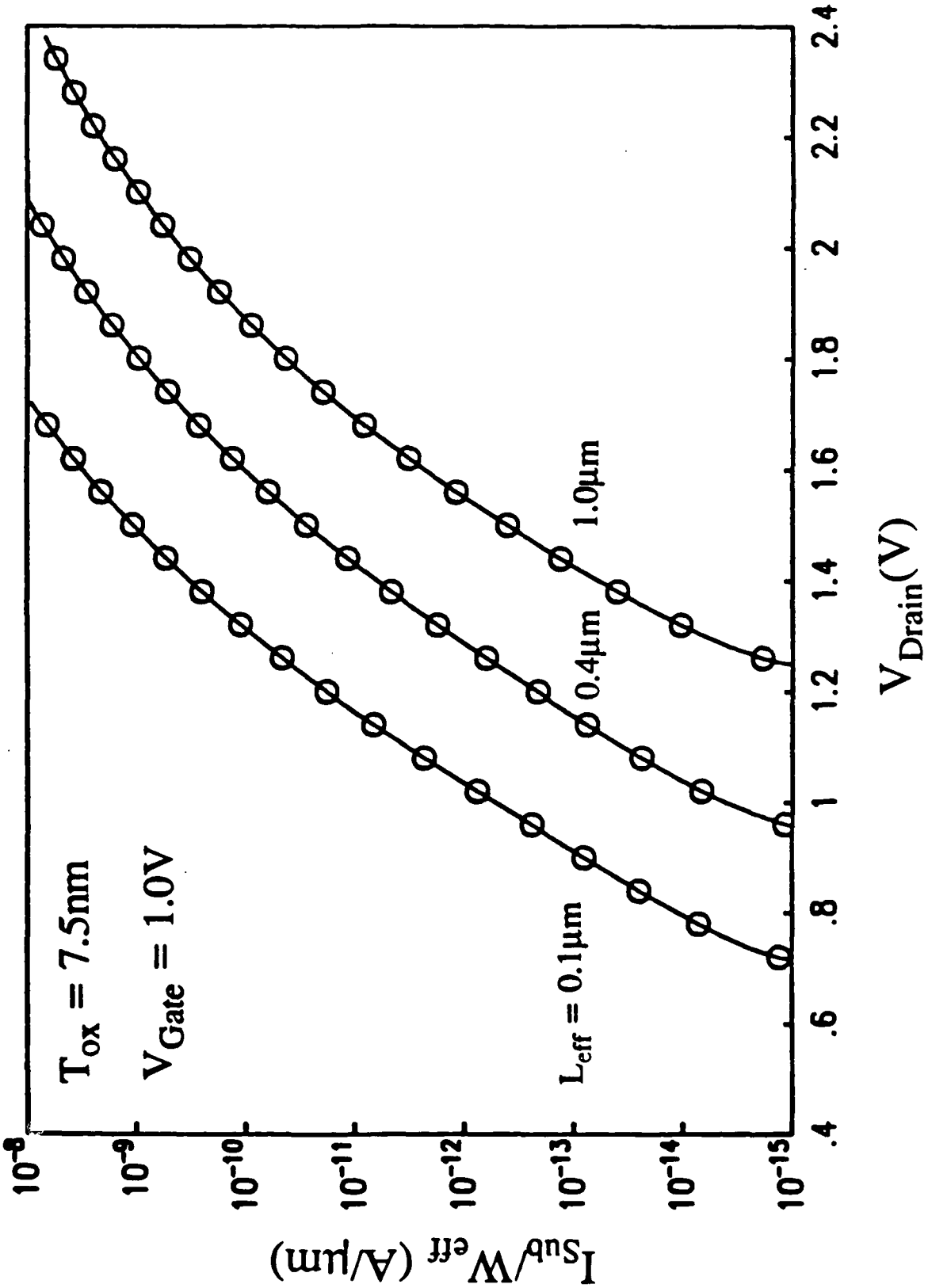
I_{Sub}/W_{eff} (A/μm)
10^{-8}
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
10^{-14}
10^{-15}
T_{ox} = 7.5nm
V_{Gate} = 1.0V
L_{eff} = 0.1μm
0.4μm
1.0μm
.4
.6
.8
1
1.2
1.4
1.6
1.8
2
2.2
2.4
V_{Drain}(V)

FIGURE 1

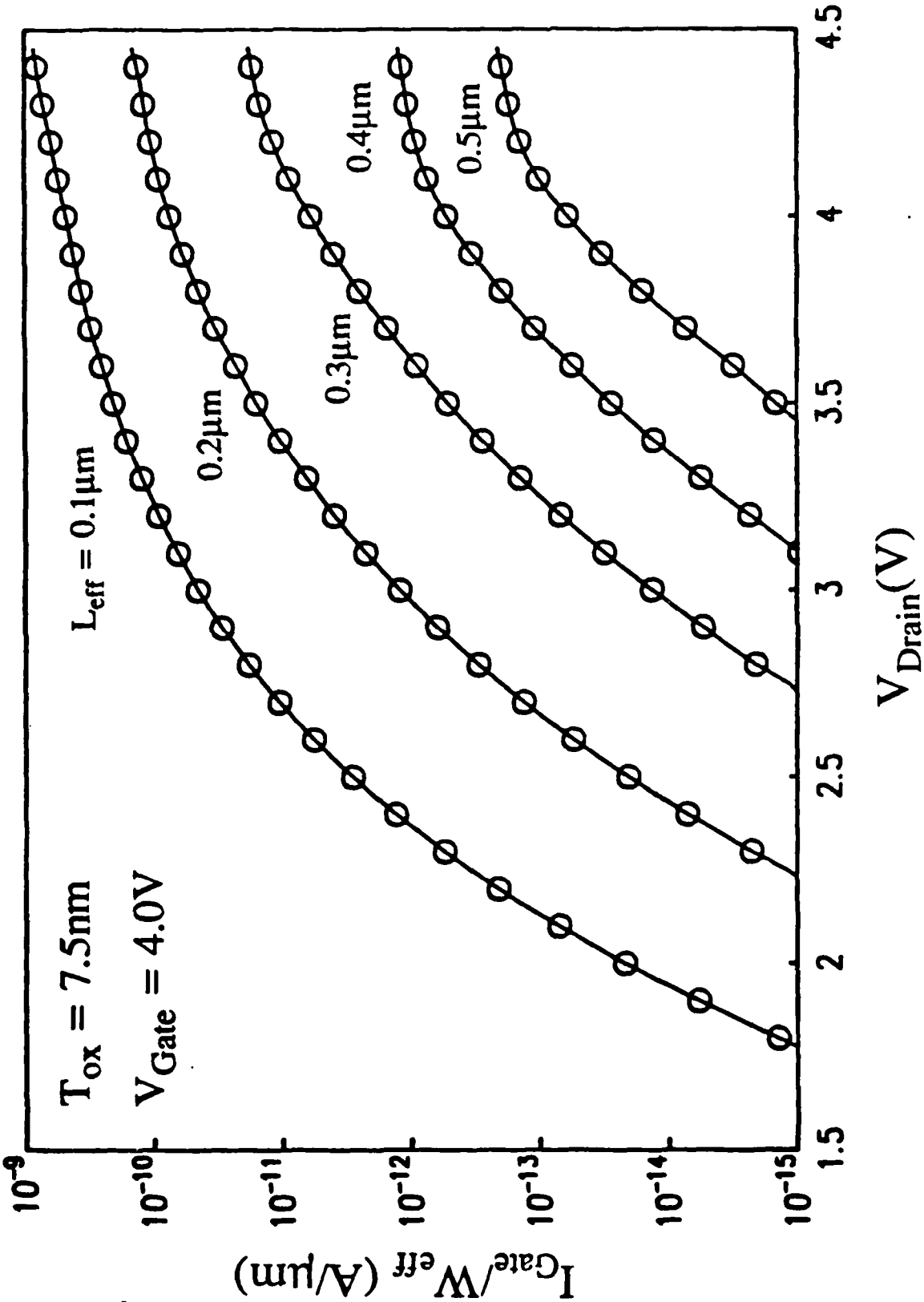
I_{Gate}/W_{eff} (A/μm)
10^{-9}
10^{-10}
10^{-11}
10^{-12}
10^{-13}
10^{-14}
10^{-15}
1.5
2
2.5
3
3.5
4
4.5
V_{Drain}(V)
T_{ox} = 7.5nm
V_{Gate} = 4.0V
L_{eff} = 0.1μm
0.2μm
0.3μm
0.4μm
0.5μm

FIGURE 2

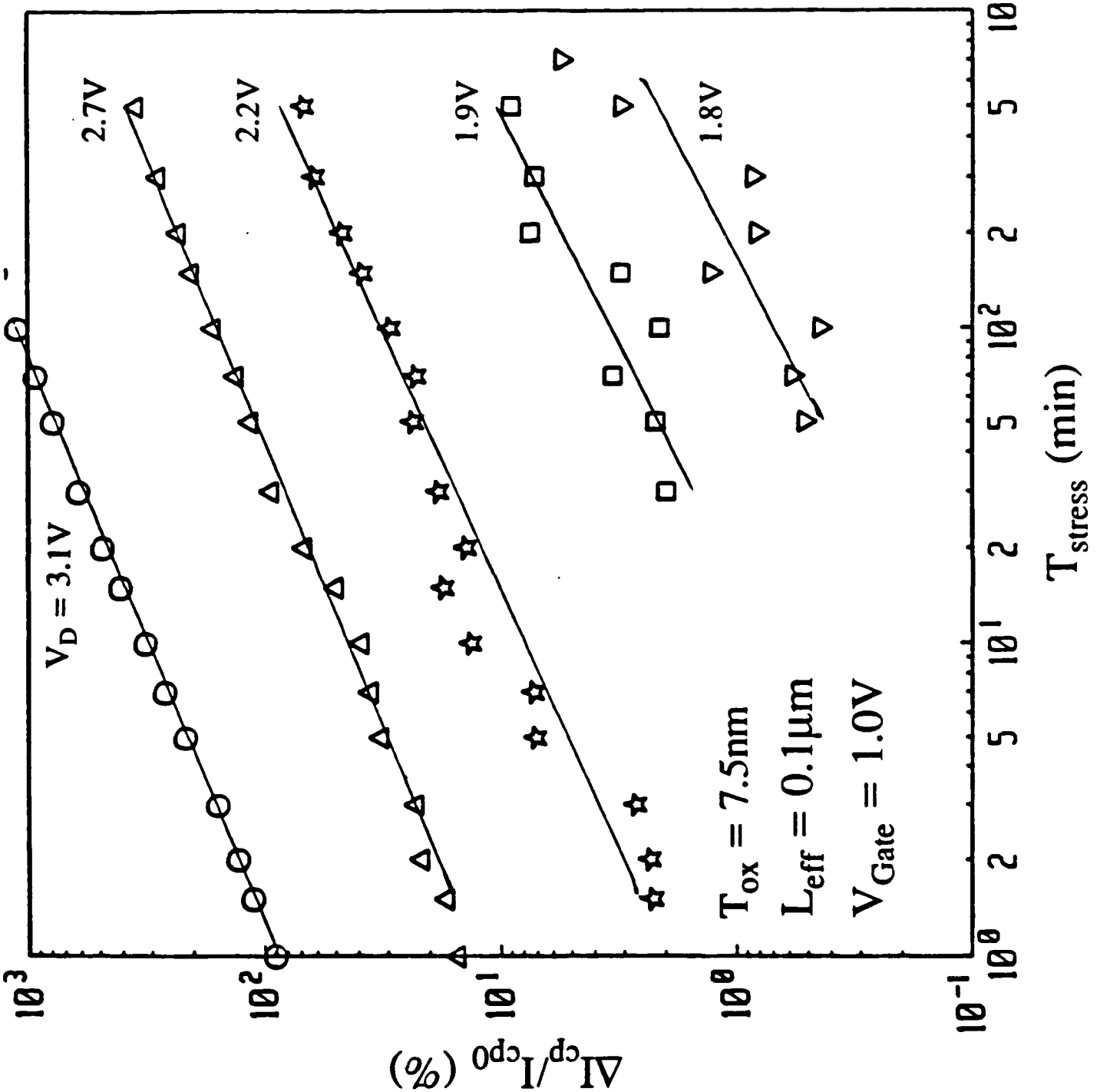
$\Delta I_{cp}/I_{cp0}$ (%)
10^3
10^2
10^1
10^0
10^{-1}
10^0 2 5 10^1 2 5 10^2 2 5 10^3
T_{stress} (min)
$V_D = 3.1V$
2.7V
2.2V
1.9V
1.8V
$T_{ox} = 7.5nm$
$L_{eff} = 0.1\mu m$
$V_{Gate} = 1.0V$

FIGURE 3

Improvements in Power and Efficiency of Planar Oscillators

Professor S.E. Schwarz with Jenngang Tsay and Mark Prouty

Advanced microwave and millimeter-wave electronic systems are moving from conventional waveguide structures toward modern integrated-circuit technology. Systems such as integrated circuit radars now appear to be possible. As compared with conventional radars, systems built on one or a few semiconductor chips can be expected to be smaller, cheaper, and more rugged. Many important applications for such tiny radar systems can be imagined.

One problem in designing miniature radar systems is that of obtaining sufficient transmitter power. The power of semiconductor device oscillators is limited, and tends to decrease rapidly as frequency increases into the millimeter-wave range. We are studying a new technique for improvement of these oscillators. We have found a technique by means of which the output power of various devices can be increased. The potential improvements are quite large in many cases. At present our studies are concentrating on Gunn diode oscillators, and we refer to the new devices as "Multi-domain Gunn Diodes." [1]

To see what improvements in power can be expected, we refer to Figure 1. This figure applies to the case of cw operation of GaAs devices, and compares output power of conventional single-domain devices with multi-domain devices having two, three, or four domains. (The derivation of this figure will be found in reference [1]. Specific assumptions have been made about geometry and heat-sinking, but the conclusions are general.) For each value of N, power drops off as $1/f^2$ above a "turn-on frequency" that increases with N. Below the turn-on frequency power drops off due to thermal limitations; above the turn-on frequency the impedance limit is dominant. We see that potential improvement increases with frequency and is of the order of N^2, where N is the number of domains. Above 12 GHz, an improvement by a factor of 4 can be obtained (as compared with conventional Gunn diodes) by using a 2-domain device. Above 30 GHz, an improvement by a factor of 9 can be had, using three-

domain devices; above 55 GHz, an improvement by a factor of 16 can be had, using 4-domain devices, and so on. It is interesting that it is at the highest frequencies, where conventional solid-state sources work most poorly, that the greatest improvements can be obtained. The high-frequency limitations of the proposed multi-domain devices are probably the same as those of conventional Gunn devices, so they will probably be useful up to more than 100 GHz. Thus they open the way to greatly increased transmitter power for compact solid-state radars in the millimeter regime.

High-power, short-pulse operation of multi-domain devices has also been investigated. Briefly, pulsed operation makes it possible to obtain improvements like those of Fig. 1, but without the thermal limitation that occurs below the turn-on frequencies. This makes it profitable to use more domains at a given frequency, with power increasing as N^2. At high frequencies, very large increases in peak power can be obtained. In present technology, pulsed operation is common only below about 30 GHz, because it relies on the efficient LSA mode of operation, which is only useful at low frequencies. Conventional transit-time devices are limited by the impedance limitation, and can produce not much more power in pulsed operation than in cw. In contrast, the multi-domain devices discussed here are transit-time devices, and will work to 100 GHz or above; however they avoid the impedance limitation. For example, a 30-domain GaAs device operated at 90 GHz, with pulse length 27 μsec and duty cycle of 0.02, should provide a peak output of 20 watts! This is about 60 times larger than the best pulsed output power available from conventional devices at this frequency.

Publications

[1] J.G. Tsay, S.E. Schwarz, S. Raman, and J.S. Smith, "Multi-Domain Gunn Diodes." To appear in Microwave and Optical Technology Letters, February 1990.

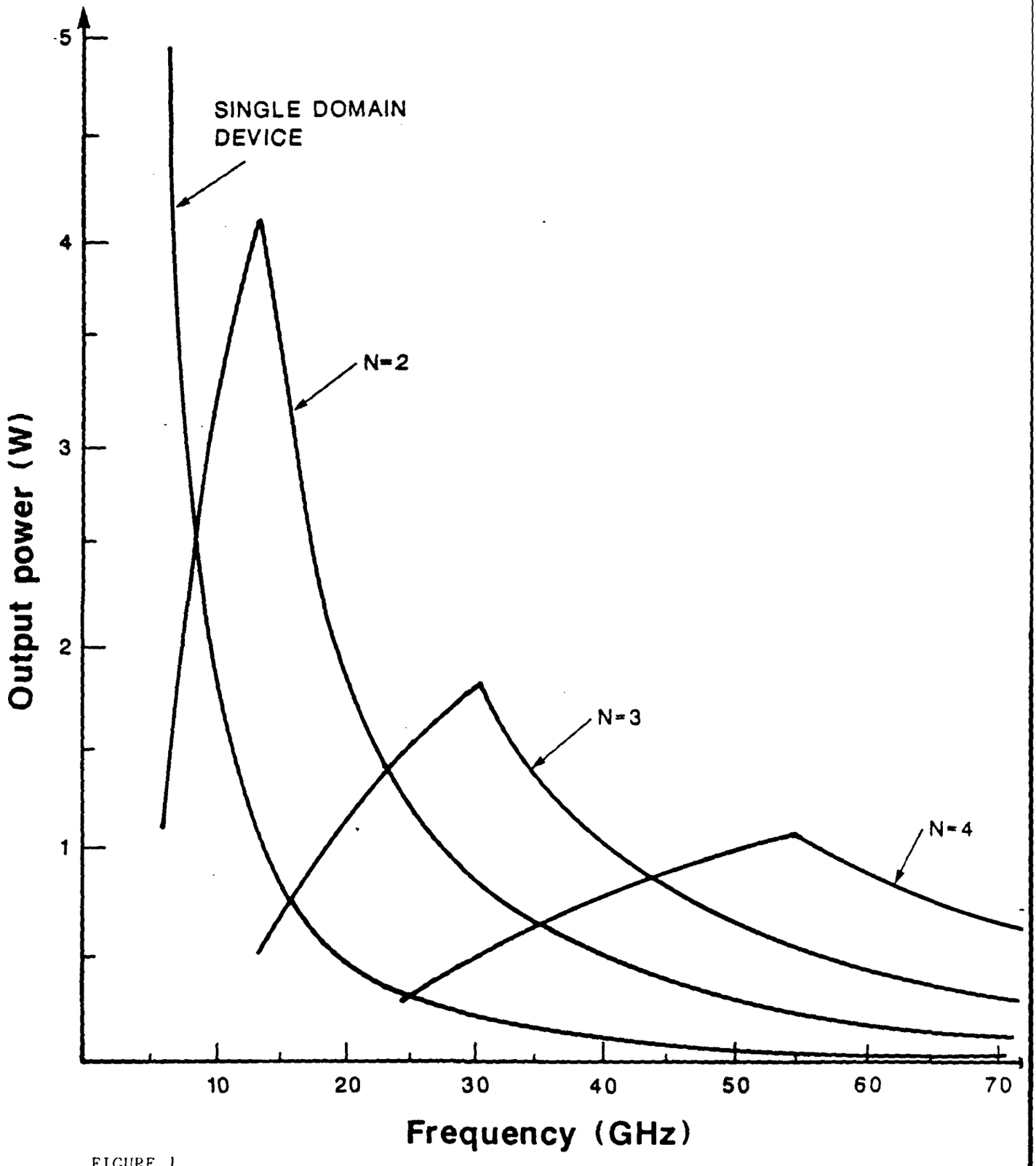
SINGLE DOMAIN
DEVICE
N=2
N=3
N=4
Output power (W)
Frequency (GHz)
1
2
3
4
5
10
20
30
40
50
60
70

FIGURE 1

Guided-Wave Nonlinear Optics

Professor S. Wang with Daryoosh Vakhshoori

Nonlinear optics based on interaction of counter-propagating waves in dielectric guides offers some unique capabilities and possibiities which are unattainable in the conventional scheme employing collinear interaction of waves. The unique features originate from the basic physics that the frequency up-converted signal emits from the surface and that it depends on the spatial variation of the two interacting waves. Utilizing these features, we have accomplished the first demonstration of:

- A guided-wave correlator capable of measuring the width of an optical pulse down to 100fs range.

- A guided-wave spectrometer capable of resolving modes of a few angstroms apart in a guide of 1 mm in length.

- Scannability of the exit angle of the frequency up-converted beam through tuning the frequency of one of the interacting beams.

We have opened a new frontier for future exploration of guided nonlinear optics. One exciting possibility is the use of the nonlinear effect as a scientific tool to study internal stress in hetero-epitaxial films by measuring modal dispersion caused by elasto-optic effect. Because of its surface emitting nature, the scheme offers an extremely interesting possibility of incorporating a superlattice to provide a suitable reciprocal lattice vector for phase matching, which will lead to the generation of coherent radiation in the visible region and beyond. We should emphasize that our scheme for guided-wave nonlinear optics is applicable to II-VI compounds as well as III-V compounds.

Fault Tolerance in Artificial Neural Networks

Read Clay with Professor C. H. Séquin

In our examinations of different strategies for overcoming hardware failures in artificial neural networks, we found a technique that can train a network to correctly respond to faults not previously seen by the network. A failure is defined as one or more hidden units that output a single fixed value (anywhere within normal output range) regardless of its inputs.

For the network to continue to function correctly after failure of one or more hidden units (with NO additional training), hidden units are randomly 'disabled' for some fraction of the pattern presentations during a standard backpropagation training phase. We found that the network could be trained with one, two, or more hidden units disabled per pattern presentation and that such training would render the network robust to single, double or multiple failures of hidden units. Furthermore, the significant and more surprising result is that prolonged training in the single-fault mode can achieve fault tolerance even with respect to multi-fault patterns for which the network has not been trained specifically. In other words, extended training while disabling only one hidden unit at a time made the network robust to not only single-unit failures, but also to two, and even three hidden units failing simultaneously. This result was found to hold for neutral failures (i.e. output clamped to the middle of the range of possible values) as well as for extreme-valued failures (i.e. output clamped to +1 for a unit with a range of -1 to +1), although somewhat longer training times are required in the latter case.

PART C - INDIVIDUAL WORK UNITS

THEME I - HIGH-SPEED WIDE-BAND ELEMENTS FOR HIGH-FREQUENCY ELECTRONICS

HFD.1. High Speed/Frequency GaAs and Si Device Research

Ultra-short Channel Devices
Professors C. Hu and P. Ko with James Chung, Jian Chen, and Peter George

In 1989 we have exploited our "resist-ashing" technique for fabrication of a very short channel transistor developed last year under the JSEP program to study the physics of ultra-small silicon devices. We have also completed several modeling studies for GaAs field effect transistors.

In one study [1] hot-electron degradation in deep submicrometer MOSFETs at 3.3V and below is studied. Using a device with L_{eff} = 0.1μm and T_{ox} = 75 angstrom, substrate current is measured at a drain bias as low as 0.7V; gate current is measured at a drain bias as low as 1.75V. Using the charge-pumping technique, hot-electron degradation is also observed at drain biases as low as 1.8V. These voltages are believed to be the lowest reported values for which hot-electron currents and degradation have been directly observed. These low-voltage hot-electron phenomena exhibit similar behavior to hot-electron effects present at higher biases and longer channel lengths. No critical voltage for hot-electron effects (such as the Si-SiO_2 barrier height) is apparent. Established hot-electron degradation concepts and models are shown to be applicable in the low-voltage deep submicrometer regime. Using these established models, the maximum allowable power supply voltage to insure a 10-year device lifetime without using LDD is determined as a function of channel length (down to 0.1μm) and oxide thickness.

We are in the process of measuring mobility in these short channel MOSFET for evidence of velocity overshoot, whose existence in these type of devices is quite uncertain. Toward that goal we have developed a technique for extracting the intrinsic transconductance [2]. As device dimensions approach the deep-submicrometer range, conventional methods of

correcting for the source-drain resistance effect must be reexamined. Significant error in the extracted g_m can arise from source-drain resistance asymmetry. A simple procedure is outlined to either correct for or to avoid this source of error. Using deep-submicrometer devices, experimental results are presented to demonstrate the severity of the potential error and to verify the applicability of the proposed technique. A method is also demonstrated which extracts the individual values of the source R_S and drain R_D resistances.

About one year ago, we discovered strong band-to-band tunneling current in small Si MOSFETs under the JSEP program and have now extended the study to the resultant hot-hole-injection gate current.[3] PMOSFET hot-carrier effects are dominated by hot electron (not hole) injection and trapping. We have modeled the electron injection current in PMOSFET. [4,5]

We have developed a circuit simulator that can simulate the response of GaAs ICs to the single-event or pulse radiation disturbances. The starting point is the development of a generalized circuit model for GaAs MESFETs.[6] The novel features of the model include continuous descriptions for the intrinsic FET, Schottky diode and inter-electrode capacitance, valid both above and below device threshold. The model also displays good agreement with HEMT characteristics. The FET model is then modified for the simulation of the effects of single-event and radiation phenomena on the operation of GaAs MESFETs. The model can be utilized in a circuit simulator to evaluate integrated circuit designs and aid in the provision of adequate upset margins for various operating environments. Additional sub-circuit construction is unnecessary since the electrical responses to the different phenomena are intrinsic to the device template. Companion models for a dielectric capacitor and an implanted resistor, that can be used to evaluate the effects of some of the above phenomena on device and circuit operation have been developed and implemented in a GaAs circuit simulator.[7]

The simulation approach adopted here departs from the commonly used sub-circuit method. The device sparse matrix template is computed in terms of an environmental variable called flux which is specified by the user. This approach allows the simulation of changes induced in the internal device parameters like threshold voltage, mobility and effective doping and also eliminates the need to maintain different device templates and additional sub-circuit elements to mimic different phenomena.

We are presently studying the hot electron effect and its role in backgating using analytical modeling and 2D device simulation. A calculation of the channel-substrate space charge densities and dimensions is required in the formulation of device models for modern GaAs FETs which are fabricated on semi-insulating substrates with multiple deep levels. We have described a procedure to deduce this information from the compensation scheme utilized to obtain semi-insulating behavior.[8]

Publications

[1] J. Chung, M.C. Jeng, J.E. Moon, P.K. Ko, and C. Hu, "Low-Voltage Hot Electron Degradation in Deep Submicrometer MOSFETs," *1989 International Reliability Physics Symposium Proceedings*, Phoenix, AZ, April 1989, pp. 92-97.

[2] J. Chung, M-C. Jeng, G. May, P.K. Ko, and C. Hu, "Intrinsic Transconductance Extraction for Deep-Submicron MOSFETs," *IEEE Trans. Electron Devices*, Vol. 36, No. 1, January 1989, pp. 140-142.

[3] J. Chen, T.-Y. Chan, P.K. Ko, and C. Hu, "Gate Current in Off-State MOSFET," *IEEE Electron Device Letts.*, Vol. 10, No. 5, May 1989, pp. 203-205.

[4] T.C. Ong, P.K. Ko, and C. Hu, "P-MOSFET Gate Current and Device Degradation," *Proceedings of 1989 International Symposium on VLSI Technology, Systems and Applications*, Taipei, Taiwan, May 1989, pp. 193-196.

[5] T.C. Ong, K. Seki, P.K. Ko, and C. Hu, "P-MOSFET Gate Current and Device Degradation," *1989 International Reliability Physics Symposium Proceedings*, Phoenix, AZ, April 1989, pp. 178-182.

[6] P. George, P.K. Ko, and C. Hu, "A GaAs MESFET Model for Circuit Simulation," *International Journal of Electronics*, Vol. 66, No. 3, March 1989, pp. 379-397.

[7] P. George, P.K. Ko, and C. Hu, "Simulating the Effects of Single-Event and Radiation Phenomena on GaAs MESFET Integrated Circuits," *Proceedings of IEEE 1989 Custom Integrated Circuits Conf.*, San Diego, CA., May 1989, pp. 9.7.1-9.7.4.

[8] P. George, P.K. Ko, and C. Hu, "Modeling the Substrate Depletion Region for GaAs FETs Fabricated on Semi-Insulating Substrates," *Solid State Electronics*. Vol. 32, No. 2, February 1989, pp. 165-168.

Improvements in Power and Efficiency of Planar Oscillators
Professor S.E. Schwarz with Jenngang Tsay and Mark Prouty

This research is concerned with oscillators for use in microwave and millimeter-wave planar circuits. Planar technology can now be used in place of older waveguide technology, resulting in improvements in size, cost, and durability. An important and expected advance in this art will be the use of miniaturized radar systems constructed on one (or a few) semiconductor chips. Such radars will be very small as compared with conventional waveguide-based systems, and can have cost advantages as well. In order to construct such systems, high-power planar signal sources will be needed. We are working on improvements in these sources.

The power of Gunn oscillators in generally limited by two factors: (a) impedance-matching problems, leading to circuit losses, and (b) thermal limitations. The important limitation in our work is the former, which gives rise to the $1/f^2$ rolloff with increasing frequency. Somewhat surprisingly, thermal effects are only important at relatively low frequencies below 10 GHz. The reason for this is that at high frequencies, impedance-matching considerations reduce the power level so much that thermal limits are not reached. In the approach being followed here, the impedance-matching limit is relaxed, increasing power levels until thermal heating enters as the ultimate limit.

The impedance-matching limitation arises because the impedance the Gunn device sees looking into the circuit must be equal to the negative of its own impedance. The voltage across the Gunn device needed for optimum efficiency at any given frequency is basically

fixed. To increase the device power, therefore, one needs to increase its current, by increasing its cross-sectional area. As we do this, the device impedance decreases, and the circuit impedance must decrease with it. But the range of impedances that the circuit can present is limited by its Q. As a rule of thumb, an impedance less than 5 ohms is hard to achieve. This problem gets worse at higher frequencies, because increasing losses cause the circuit Q to decrease. It is also a greater problem in MMICs than in the older waveguide-based circuits, again because available Qs are limited. Thus one reaches a maximum size for the Gunn diode. Typically the device voltage goes down as $1/f$; to keep device impedance constant the current, and therefore the device area, must also be reduced as $1/f$. Thus the power (proportional to vi) goes down as $1/f^2$.

Already many years ago, it was realized [H.W. Thim, 1968] that the $1/f^2$ limit could be avoided if several devices were connected in series. This has the effect of increasing the impedance level: if N devices are used in series the current remains the same but the voltage and the impedance are multiplied by N. It is probably not feasible to place the diodes far apart, because the parasitics associated with the interconnections would interfere with circuit operation. However, it should be possible to obtain true series operation if the devices are placed directly one on top of the other. In fact, this technique was successfully demonstrated at very low frequencies (1.3 and 2.5 GHz) by Thim in 1968, using a primitive technique in which several wafers, each 40 microns thick, were stacked one upon another.

Although the idea is old, and has even been demonstrated to work, it seems to have been largely given up in recent years. Little has been published about it, but there are rumors of unpublished attempts. It appears that efforts at stacking several diodes one upon another, as Thim did, have been unsuccessful at higher frequencies. One can imagine why this might be. High-frequency diodes are very small, and are usually mounted in packages. But the packages contain parasitics that intervene between the diodes and interfere with the operation of the cir-

cuit. Alternatively, one might try simply stacking several chips one on top of the other, inside a single package. However, this is a difficult task mechanically, because the chips are less than 100 microns square. Moreover, the chips are thicker than the devices themselves, because of the substrate thickness. The additional thickness would act as an impedance for heat flow and thus lead to excessive thermal rise.

We are attempting to avoid these difficulties and successfully apply Thim's approach at high frequencies by taking advantage of modern epitaxial technology. That is, we suggest that all the diodes can be fabricated together, one on top of the other, in a single monolithic unit, by means of molecular beam epitaxy (MBE). This eliminates the need for interconnections, while taking advantage of MBE's high precision to obtain the required doping profiles. The resulting series arrays of Gunn diodes will act as single devices, inside which several domains simultaneously move, one after another, in the direction from cathode toward the anode. Thus we refer to the new devices as "Multi-domain Gunn diodes."

As in any situation in which several oscillators are locked together, it is necessary that the individual oscillators be nearly identical. If they are not, they will tend to oscillate independently at different frequencies. The accuracy of fabrication that is required, in order to make the diodes sufficiently identical, is obviously a crucial point, and we have given it considerable attention. By means of computer simulation we have determined the degree of accuracy that is required; it is well within the capabilities of MBE. It may also be objected that even if the sections of the device are identical, they will act as though they are not identical when they are at different temperatures. This effect has also been studied by simulation. It imposes a limit of about 50 degrees K on the allowable temperature difference inside the device. This limit is important, but fortunately it sets in only at power levels much higher than those of existing devices.

As a typical indication of what we believe can be achieved, let us consider the case of cw operation of a GaAs device at 30 GHz. In publication [1] below we have shown that a 3-domain device should produce 1.8 W of output power. A conventional single-domain device, under the same assumptions, would produce only 0.2 W. The improvement over conventional devices is expected to increase further as frequency increases, up to a limit (for GaAs Gunns) approaching 100 GHz. High-power, short-pulse operation of multi-domain devices has also been investigated. In this case very large increases in peak power can be obtained. For example, we predict that a 30-domain GaAs device operated at 90 GHz, with pulse length 27 microsec and a duty cycle of 0.02, should provide a peak output of 20 watts. This is about 60 times larger than the best pulsed output at this frequency from conventional devices.

An interesting feature of the proposed technique is that it can be applied in a great variety of applications. For instance, it should be just as useful with InP devices as with GaAs, and it will be beneficial in pulsed operation as well as in cw. Although it is not the focus our present work, it will probably work with pulsed IMPATTs as well. Furthermore, it is compatible with other work involving diode arrays. At present, various workers are studying the use of power-combining techniques, in order to obtain greater powers than can be had from a single diode. The approach proposed here will be useful in that kind of work too; one can do power-combining of the multi-domain devices we propose. By constructing power-combined arrays of multi-domain diodes, which are already powerful by themselves, output powers that are really awesome (by semiconductor device standards) should be obtainable.

In related work, we are also studying losses in the resonant circuits used in planar oscillators. These resonators are still not well understood. Because they are open structures they exhibit radiation loss, which at high frequencies can become large. This can cause an oscillator's output power to be reduced to a much a greater degree than one might expect. A computer study of radiation losses from planar resonators is being performed. The approach

being taken is different from what has been done before: a Green's function for the radiation and surface-wave fields is constructed by means of reciprocity. Experiments measuring Q of these resonators are also being performed, using artificial dielectric materials near 1 GHz. The theory is being tested on conventional half-wavelength straight microstrip resonators. Once it has been verified we plan to design improved resonators with reduced loss.

Publications

[1] J.G. Tsay, S.E. Schwarz, S. Raman, and J.S. Smith, "Multi-Domain Gunn Diodes," to appear in *Microwave and Optical Technology Letters*, February 1990.

HFD.2. GaAs/Si Devices and Materials Studies

Professor S. Wang with H.P. Lee

Our research efforts during 1989 are focused on two subjects: (a) use of modulation MBE and strained layer superlattices for improving the crystalline quality of GaAs/Si and GaAs/InP films and (b) studies of DH GaAs/GaAlAs lasers on Si substrates. We are pleased to report that our efforts have yielded positive results towards two-dimensional growth of hetero-epitaxial films and stress relief in the grown films.

In the previous progress report, we introduced a new growth technique the modulated MBE, using a pulsed As beam. This is accomplished by opening and closing the As shutter at an interval of 3 seconds, approximately the time for two-monolayer growth of GaAs to allow surface migration of Ga atoms in the absence of As flux. Buffer GaAs films of about 100 angstrom and 150 angstrom were grown by this technique at a substrate temperature of 300°C and 370°C respectively. For comparison, identical procedure was used to grow GaAs films by the conventional two-step MBE.

Plan-view TEM pictures show clear Moire interference fringes due to the presence of nucleated GaAs films on the Si host substrates [1,2]. For the samples grown by conventional MBE, the Moire pattern indicates disjointed islands of nucleated GaAs films. For the samples grown by modulated (or migration enhanced) MBE, the Moire fringes are streaker, much narrower, and more uniform. These features indicate a strong tendency toward 2-dimensional growth. Cross-sectional TEM pictures taken from the same samples corroborated this conclusion, showing uniform, 2-dimensional growth in the modulated MBE case and lumpy, island growth in the conventional MBE case [3,5].

While the thin films were used in our study of initial nucleation of heteroepitaxial GaAs films on Si substrate, thicker films were used for measuring photoluminescence spectra and X-ray rocking curves. For the thick GaAs on Si films, an initial buffer layer of 1,000 angstrom

was grown by both methods. Then the growth was interrupted. Following in-situ annealing by raising the substrate temperature to 620°C for 10 minutes, growth was resumed by normal MBE for a total thickness of 3 μm. The modulated-MBE grown films show a much stronger PL signal (by a factor of 2) and a much narrower X-ray diffraction width (250 versus 310 arc second) [3,5]. These studies clearly show significant improvement of film quality in relatively thick GaAs films needed for device fabrication.

It is known that 3-dimensional GaAs islands are first formed at the steps of the mis-oriented Si substrate. When the island thickness exceeds the critical value, misfit dislocations are generated at the top of the islands and then glide to the hetero-interface. Since only type II dislocations are capable of such glide, 3-dimensional island growth will necessarily result in the formation of type II misfit dislocations. As the growth continues, stacking faults and threading dislocations are formed when the islands coalesce. A 2-dimensional-like nucleation, on the other hand, forces the formation of misfit dislocations to the hetero-interface due to its larger nucleation size. Therefore, we expect that type I dislocations are favored over type II dislocations (threading type) in modulated-MBE grown films [3,5]. A detailed analysis of possible mechanisms for formation and propagation of defects at and from hetero-interface can be found in [9,10].

In the previous progress report, we also presented preliminary results in GaAs/InP hetero-epitaxial films. Three buffer-layer structures under study [4] are (1) GaAs layer grown at low temperature, (2) low-temperature GaAs layer plus two sets of InGaAs/GaAs strained-layer superlattices of 5 periods each and spaced 1 μm apart, and (3) transitional compositionally graded $In_x Ga_{1-x}$ As layer from x=0.53 to x=0.08. After the buffer-layer deposition, the growth was continued by conventional MBE to a total thickness of 3 μm for all samples. The 77K photoluminescence measurements showed that the SLS sample has the highest PL intensity and the lowest PL linewidth. Cross-sectional TEM studies showed that significant bending

of the threading dislocations by the second set of SLS has taken place. Although the bending of dislocations by the first set cannot be clearly seen from the TEM picture due to the high dislocation density (10^8 to 10^9 cm^{-2}) near the interface, substantial reduction of dislocation density after the first set has been observed. The TEM and PL studies strongly indicate that SLS is effective in reducing the propagation of threading dislocations.

The purpose of modulation MBE and SLS is to control and thus minimize generation and propagation of dislocations in epitaxial films near the hetero-interface. Besides dislocation density, another important consideration is thermal stress. For semiconductor lasers, thermal stress is known to be a determining factor for operating life. Previously, we have used PL spectrum, specifically the splitting of the PL spectrum, as a measure of thermal stress in GaAs/Si films. Different amounts of splitting were observed in films grown on patterned Si substrates. We have extended the technique of selective-area growth to the fabrication of DH lasers, and observed very interesting polarization effects [6,7,8]. Three laser structures were grown: (1) planar structure with DH layers grown on planar Si substrates, (2) mesa structure with DH layers grown on trenched Si substrates and with the mesa portion used for the laser and (3) selective-area grown structure with DH layers grown in the openings of SiN masked Si substrates. Essential differences in the laser behavior are summarized below.

If the stress is uniaxial and along the length of the laser stripe, TE and TM polarizations are both perpendicular to the stress symmetry axis, and the TE mode is expected to lase first as in lattice-matched DH lasers because the TE mode has a slightly larger mirror reflectivity than the TM mode. If the stress is uniformly biaxial, say $\sigma[0\ 1\ 1]=\sigma[0\ \bar{1}\ 1]$, then the TM mode is expected to lase first because the matrix element M^2 for polarization parallel to the stress symmetry axis is larger than that for polarization perpendicular to the stress symmetry axis. In planar, stripe lasers with the Si substrate thinned down to 100 μm, there is significant bowing in the longer dimension, which relieves the thermal stress in that direction. Therefore TE polar-

ization is stronger in narrow stripe (3-5 μm) lasers [6,8]. In selective-area grown, stripe lasers, on the other hand, bowing is much reduced possibly due to the presence of the SiN mark. Therefore, TM polarization is stronger [6,8]. For mesa stripe lasers with 3 to 5 μm stripe width and aligned along [0 $\bar{1}$ 1] direction, the polarization is predominantly TE, indicating a substantial relief of stress in the lateral direction and thus an almost uniaxial stress [7,8]. The planar stripe laser after thermal annealing and the mesa stripe laser show very similar polarization characteristics (strong TE) as the homoepitaxial GaAs/GaAs laser. The differential quantum efficiency of these lasers varying from 18% to 29% is also comparable to that of the homoepitaxial laser.

In summary, the two fundamental problems we face in hetero-epitaxial films grown on lattice-mismatched substrates are high dislocation density and high thermal stress. We have shown that modulation MBE promotes two-dimensional growth and SLS prevents threading dislocations from propagating. Therefore, the two approaches are effective in reducing dislocation density in heteroepitaxial films near the hetero-interface. We have also shown that substrate thinning and mesa structure are effective in relieving thermal stress in one direction in planar-structure and mesa-structure lasers. However, uniaxial thermal stress remains in these lasers, limiting the operating life of these lasers. Possible approaches to overcome this problem include low temperature growth and use of quantum well. Three problems were encountered with the selective-area-grown laser. First, the poly-crystalline GaAs grown on the SiN mask makes it very difficult to cleave the laser. This problem can be solved by using RIE instead of cleaving to form a laser cavity. Second, the RIE used to open windows in SiN mask for selective growth seems to have destroyed the slight misorientation of the exposed Si substrate surface [6]. This problem negates the benefit of modulated MBE and needs to be addressed. Third, the selective-area-grown laser does not show significant relief of thermal stress when the substrate is thinned down. The differences between the structure of this type of laser and those

of the two other types are the presence of polycrystalline GaAs in the masked region and the proximity of SiN to the active layer. The inability of the structure to relieve thermal stress needs further study to determine whether the problem can be overcome.

Publications

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[8] X. Liu, H.P. Lee, and Shyh Wang, "Polarization Effect by Intrinsic Stress of AlGaAs/GaAs DH Lasers on Si Substrate," submitted for publication to *Applied Physics Letters*.

[9] H.P. Lee, "Material and Device Studies of Heteroepitaxial GaAs Films on Si Substrates by Molecular Beam Epitaxy," Ph.D. Thesis, University of California, Berkeley, November, 1989.

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Phase-Locked Epitaxy
Professor J. Stephen Smith with Hong Lin, Jeff Walker and Sol Dijaili

We have developed a method which is generally applicable to synchronization of an electrical pulse train with an optical pulse train, such as that generated by a CPM laser. Central features include a pulsed optical phaselock loop that utilizes a gain switched semiconductor laser which is cross correlated with the femtosecond pulse train at its leading edge. We have achieved 50 femtosecond time jitter between the two pulse trains with an effective averaging of over one millisecond. This unique pulsed optical phaselock loop (POPLL) is a key component of our new subpicosecond optical sampling system.

We have succeed in using fundamental characteristics of MBE growth in a simple technique which combines the advantages of phase-locked epitaxy, short-period superlattices, and growth interruptions, to control the layer periodicity, interface flatness, and producibility of structures. Fabricated multiple layer reflectors show dramatic improvement in grown layers, with experimental reflectance spectrum showing an extremely square stop band and very regular side lobes closely matching the theoretical spectrum. A comparison of experimental to theoretical reflectance spectra is used to show that the layer periodicity is maintained within 1% and the interface flatness controls the optical loss per interface to less than 0.1%. Experimental results show a maximum reflectance of 98.5% for a $(GaAs)_3(AlAs)_6/(GaAs)_4(AlAs_1$ 35.5 period Bragg reflector.

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Papers

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[3] J.S. Smith, D. Vakhshoori, J. Walker, S. Dijaili, and S. Wang, "Integrable Parametric Waveguide Spectrometer-A Nonlinear Optical Device Capable of Resolving Modes of Semiconductor Lasers," *Applied Physics Letters*, Vol. 55, No. 12, pp. 1164, September 1989.

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HFD.3. Basic Techniques for Electromagnetic Scattering and Radiation

Superabsorption Boundary Conditions and High Order Finite Difference Methods in Time Domain Solutions of Maxwell's Equations

J. Fang and Professor K.K. Mei

For some time investigators in time domain computations of Maxwell's equations for radiation problems have been using Yee's lattice for the finite difference equations and Engquist and Majda's absorbing boundary conditions for radiation conditions. They are indeed good methods and we have gotten a lot of mileage out of them.

As the applications of time domain computation are extended to ever larger problems and as the accuracy demands of the solutions become more stringent both the Yee's method and Engquist and Majda's condition become less than adequate. For Yee's equations, the numerical dispersion becomes significant after 1,000 time step computations and for Engquist and Majda's condition the reflection error needs to be further reduced when solving microwave circuit problems.

In this research we have investigated the high order finite difference to reduce numerical dispersion and created the "Super-absorption" technique to reduce reflection error. We have thus advanced the art of time domain computation to a new level.

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Electromagnetic Properties of Superconductor Surfaces
Professors K.K. Mei and T. Van Duzer with Guo-chun Liang

With the present pace of research and development activities in superconductors, the superconductor boundary value problem is suddenly a "hot" subject. To pursue this study, the electromagnetic behavior of a superconducting medium must be clearly understood. If a superconducting surface were a lossless surface (as it is at T=0), it would be electromagnetically almost indistinguishable from a perfecting conducting surface except that magnetic field can penetrate into the superconductor with very small penetration depth (typically 100 nm). However, at microwave frequencies and $T \neq 0$ a superconductor is not a lossless material, the loss is, in fact, proportional to frequency squared.

In this project, we have studied the factors that distinguish superconductors from normal materials and developed advantageous ways of handling boundary-value problems. A superconducting material is more conveniently treated for boundary-value problems as a dielectric material with negative real part of the dielectric constant for boundary-value problems. By considering a superconductor as a generalized dielectric material, some electromagnetic problems are simplified. Since the dielectric parameter is an integral part of electromagnetic computation, it does not present any technical difficulty to existing computer programs if the dielectric constant passes from a positive value to a negative one.

The generalized dielectric constant method is rather direct. First we find the complex dielectric constant of the superconductor by using the two-fluid model or the Mattis-Bardeen formula so that we can treat the superconductor as a lossy dispersive dielectric material. By using this method, we have successfully explained the existing electromagnetic properties of superconductors, such as the Meissner effect. We have also investigated superconductive surfaces, superconductive microstrip lines and superconductor-coated waveguides. Comparisons between normal-metal transmission lines and those made of superconductors indicate a significant difference in propagation properties; superconductor transmission line has much low

loss and less dispersive.

As a consequence of this electromagnetic treatment of a superconductor, the existence of a surface wave on a superconducting surface is also predicted. It is more tightly bound to the surface than are surface waves on normal metals.

In addition we have developed a time-domain computational method involving dispersive media, such as superconductors or plasmas. The method involves a time-domain finite-difference technique with a system-function expansion, so that no explicit convolution is required. It thus greatly reduces memory demand and CPU time.

Publications and Papers:

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[2] K. K. Mei, G. C. Liang, and T. Van Duzer, "Electromagnetics of Superconductors," in preparation to be submitted for publication.

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HFD.4. Submillimeter-Wave Mixing with Superconductive Tunnel Junctions

Professors Theodore Van Duzer and Paul Richards with Michael Bruns

Submillimeter-wave mixing with superconductive tunnel junctions offers the opportunity for the greatest sensitivity possible for any type of mixer. There is a sound theoretical base and a number of experimental verifications. It is well known that this very sensitive detecting device has the disadvantage that it easily saturates; we have therefore concentrated on the idea of using series arrays of junctions in which the dynamic range increases a n^2, where n is the number of junctions in the array. We have sought to develop a rugged, controllable technology for making series arrays of tunnel junctions. It is also desirable to make a thin-film antenna connected directly to the junction array.

The fabrication process is an adaptation of the superconductive niobium circuit process developed in our laboratory for making larger junctions for digital integrated circuits in which the junctions are formed by a subtraction process from a whole-wafer junction. The patterning used for the small 1 μm^2 mixer junctions is different from that used for the larger ones; here the square junction is patterned by the intersection of two 1 μm-wide lines in two separate processing steps. The focus of the effort to define the junction was on an etch-and-anodize process. The counterelectrode was etched by RIE and then anodization was used to form an insulating surrounding region. Similar steps have been used in other laboratories for small junctions.

The results of the project include some good 1 μm^2 junctions. The best junctions showed low subgap currents and would have been useful for mixer application. We did not gain sufficient control and repeatability to make useful arrays. Designs for three different types of thin-film antennas, bow-tie, equiangular spiral, and circular log-periodic, were produced. That part of the project has been combined in another project with a different method of making single junctions. Most of the work on this project is in the report referenced below.

Papers

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SPL.1 Electro-optic Probing of Semiconductor Materials and Devices

Nonlinear Guided-Wave Optics
Professors S. Wang and J. Steven Smith with D. Vakhshoori

In the previous progress reports, we introduced a new scheme for guided-wave nonlinear optics involving the parametric interaction of two contra-propagating waves and reported our preliminary results on a guided-wave correlator. Because the second-harmonic (SH) signal depends on the simultaneous presence of two interacting fundamental beams, one being the incident wave and the other being the reflected wave, information about the width of a laser pulse can be deduced from the spatial variation of the SH signal near the end of an optical cavity where there is a spatial overlap between the incident and reflected waves.

In the first experiment, the output from a YAG laser was compressed to a 7-ps pulse and then fed into an optical cavity. The observed spatial span of the SH signal was about 400 μm. Because the time required for the pulse to travel the whole length of the cavity is comparable to the pulse width, multiple reflections take place and account for the observed spatial span of the SH signal. An analysis of the SH signal based on double reflections at both facets gives a value of 7 ps for the YAG pulse in good agreement with the value measured by the standard auto-correlation measurement.

To eliminate the uncertainty in the value of pulse width caused by multiple reflections, we can either increase the cavity length or shorten the pulse width. We take the latter approach for the dual purpose of removing the uncertainty and demonstrating the capability of the method to measure the width of ultrashort pulses [1]. A 156-fs optical pulse from a F-center laser was used, and coupled into an optical cavity of 150- μm length. The measured spatial span of the SH signal is 5 μm, corresponding to a pulse width of 160 fs. The spatial span was broadened to 15 μm in a cavity of 800- μm length due to material and modal dispersion in the waveguide. Therefore, both effects of multiple reflections and propagation dispersion must be minimized in order to use the following formula

$$\Delta t = 2\sqrt{2}\, n(w)\Delta L/c$$

between the FWHM Δt of the optical pulse and the FWHM ΔL of the SH correlation trace.

Another important application of nonlinear optics involving two counter-running waves is a guided-wave spectrometer which translates information about far-field angle θ into wave number κ and thus wavelength λ. If the counter-running waves have the same wavelength, then the longitudinal wave vectors cancel, resulting in radiation of the SH signal normal to the surface. If they have different wavelengths, the residual wave vector in the longitudinal direction makes the SH signal to radiate at an oblique angle $\theta \neq 90°$. Therefore, if we keep the wavelength λ_0 of one laser beam fixed and vary the wavelength λ_1 of the other laser beam, then we can deduce from the exit angle θ of the frequency up-converted beam information about λ_1 (spectrometer) or have an angle-scannable frequency up-converted beam (beam scanner). We have demonstrated the wavelength dependence of the exit angle, and clearly resolved the longitudinal modes (9 angstroms apart) of semiconductor lasers (1.3 μm quaternary laser) by mixing them with a cw Nd = YAG laser beam [2]. The amount of power coupled into the optical cavity is estimated to be around 100 μw for the YAG laser beam and 50 μw for the semiconductor laser beam.

In summary, we have carried out a novel scheme for nonlinear interaction in optical waveguides involving two counter-propagating waves, and successfully demonstrated useful devices. Specifically correlators and spectrometers, which are important components for guided-wave optical communications to measure the temporal width and to monitor the spectral stability of semiconductor lasers. For the correlator, the length of the optical cavity should be properly chosen to minimize the effects of multiple reflections and velocity dispersion. For the spectrometer, the resolving power is increased with increasing cavity length and increasing mirror reflectivity. For a cavity length of 1 mm and a mirror reflectivity of 0.35, two modes separated by 4 angstroms can be clearly resolved. We are investigating a number of possibili-

ties with nonlinear interaction of counter-running waves including schemes for an efficient SH-laser for delivering power in the MW range and uses as a scientific tool for material studies, such as measuring internal stress. Further discussions of correlator, spectrometer, and other possibilities can be found in [3,4]. Finally we should mention that a paper summarizing our work on electro-optic probing was published recently [5]. The paper includes the use of electro-optic probing to measure the spatial distribution of deep-level defects possibly due to EL2 in semi-insulating GaAs.

Publications

[1] D. Vakhshoori, J. Walker, S. Wang, J.S. Smith, C.E. Soccolich and M.N. Islam, "Integrable Optical Correlator: Its Temporal Resolution, Spectral Response, and Power Sensitivity," *Applied Physics Letters*, 54 (2), May 1, 1989, pp. 1725-1727.

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Non-Contacting Magnetic Probe
Professor S.E. Schwarz with Sam Osofsky

Electro-optic probing is a possible technique for making measurements on planar high-frequency microwave and millimeter-wave circuits (MMICs). We have also been working on an alternative technique for such measurements, based on non-contacting magnetic probes.

These probes essentially act like the secondary of a transformer, responding to the magnetic field produced by current in the circuit under test. They can be positioned above any point in a circuit in order to measure the current flowing at that point. Both amplitude and phase can be measured. By maintaining the proper spacing between the circuit and the probe, coupling is maintained at a low level, so that circuit operation is not disturbed by the probe. Electrical contact between circuit and probe is not required.

For detailed studies of circuit operation, one can apply power and an input signal to a circuit (using either bond wires or a Cascade probe) and then move the magnetic probe through the circuit, determining current amplitude and phase at positions of interest. Amplitude measurements are made by simply applying the output of the probe to the input of a spectrum analyzer. Phase measurements can be also be made, by the following method. A small amount of power is derived from the input signal, passed through an adjustable phase shifter, and recombined with the probe signal by means of a directional coupler. When the setting of the phase shifter is varied, the magnitude of the spectrum analyzer's input signal will increase or decrease, owing to constructive or destructive interference. By noting the setting of the phase shifter that results in maximum combined signal we can determine the phase of the current at the point being measured. Interestingly, phase measurements are more accurate than amplitude measurements, since they do not depend for accuracy on precise positioning of the probe.

The non-contacting probes can be used as diagnostic tools for perfecting circuit design. That is, circuits can be probed to determine how closely currents at internal points agree with the designer's intentions. The design can then be modified so that ideal operation is obtained. Another potential application is production testing.

Publications

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THEME II - NEW ARCHITECTURES FOR PARALLEL COMPUTATION

MPC.1. CAD and Architectural Problems in Realizing Massively Concurrent Computation

A Novel Approach to IC Performance Optimization by Clock Routing
Professor E.S. Kuh with Arvind Srinivasan and Michael A.B. Jackson

This research was begun in the summer of 1989. The clock is the essence of a synchronous digital system. Physically, the clock is distributed from an external pad to all similarly clocked synchronizing elements through a distribution network that encompasses combinational logic and interconnects. It serves to unify the physical and temporal design abstractions by determining the precise instants in time at which the digital machine changes state. Because the clock is important, optimization of the clock signal can have a significant impact on the chip's cycle time, especially in high-performance designs. Non-optimal clock behavior is caused by two phenomena: the routing to the chip's synchronizing elements, and the asymmetric behavior of the clock distribution logic.

In this research work we focused on routing techniques for optimizing clock signals in VLSI circuits. In all previous work, the routing of the clock net has been performed using ordinary global routing tools based on a minimum spanning or minimal Steiner tree that have little understanding of clock routing problems. We present a novel approach to clock routing that all but eliminates clock skew and yields excellent phase delay results for widely ranging chip sizes, net sizes (pin count), minimum feature sizes, and pin distributions on both randomly created and industrial standard benchmarks. For certain classes of pin distributions we have proven theoretically and observed experimentally a decrease in skew with an increase in net size. In practice, we have observed a two to three order magnitude reduction in skew when compared to a minimum spanning tree.

We have developed an algorithm called the *Method of Means and Medians* for routing clock signals, given an initial placement of the synchronizing elements on the chip. The algorithm is vastly superior to standard routing techniques for widely varying region size, clock pin

distributions, numbers of clock pins and technology feature size, in terms of skew and phase delay results. Figures 1 and 2 show the clock net routing for standard MCNC benchmark examples Primary1 and Primary2.

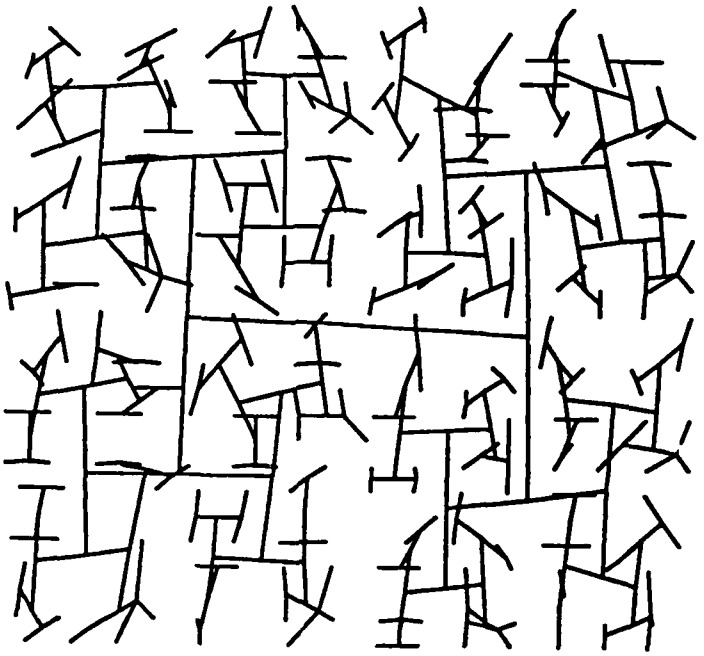

Figure 1: Primary1 clock routing

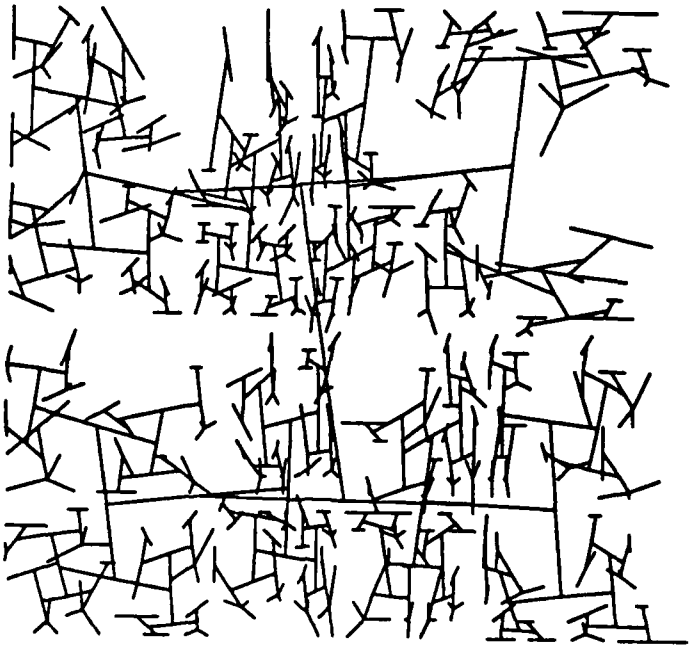

Figure 2: Primary2 clock routing

We plan to investigate introducing buffers in the clock net in order to further reduce phase delay. Also, the impact of the clock routing on chip congestion and overall wireability is being investigated. Future work will also address the possibility of combining our algorithm with a minimum spanning tree algorithm to reduce the net length of the clock net while compromising a little on the skew.

Publications

[1] A detailed paper describing the work done and the results obtained has been submitted to the Design Automation Conference, 1990.

A Massively Parallel Algorithm for Sea-of-Gates Placement
Professor E.S. Kuh with Arvind Srinivasan

The focus of this research is to develop a placement method for very large IC's that is suitable for execution on massively parallel machines. Our method is based on the work of Tsay, Kuh and Proud [1]. The method involves solving large sparse systems of equations in parallel, and the technique we used to solve them are based on the Gauss-Jacobi method. The approach uses a partitioning scheme to successively generate smaller and smaller sub-problems each of which may be solved in parallel. The run-time complexity of the algorithm is $O(n)$ using $O(n)\times d$ processors where d is the maximum connectivity of any module on the chip. This represents a speedup of $O(log\ 2n)$ over the sequential version of the algorithm.

We have implemented a preliminary version of the algorithm on the Connection Machine [2] system and are in the process of testing it on large examples.

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[2] Thinking Machines Corporation. *Using the Connection Machine System. May 1988.*

Heterogeneous Artificial Neural Network Architecture
Chedsada Chinrungrueng (Professor C. H. Séquin)

We are investigating hybrid combinations between the multilayer perceptron (MLP) and the radial basis function (RBF) architectures. These heterogeneous architectures inherit the fast convergence rate of the RBF architecture and the hardware parsimony of the MLP architecture and they still have a modular structure that is suitable for VLSI implementation. In addition, they offer intriguing possibilities for the implementation of fault tolerance.

The basic scheme of these heterogeneous architectures is to divide an assigned task into independent, simpler subtasks, and then to solve each subtask separately. Assuming that we want our system to implement an overall function $f(\mathbf{x})$, the division of this task can be achieved by decomposing this function into a collection of simpler functions

$$\{ \quad f_i(\mathbf{x}) \quad | \quad i = 1, \ldots, n \; ; \quad f_i(\mathbf{x}) = \phi_i(\mathbf{x}) f(\mathbf{x}) \quad \text{and} \quad \sum_{i=1}^{n} \phi_i(\mathbf{x}) = 1 \quad \}.$$

Each function in this collection is then approximated separately. The overall response function is a combination of the approximations of all $f_i(\mathbf{x})$. In case of simple, non-fault-tolerant analog function approximation, this amounts to simple linear summing. In order to ensure smoothness of the overall response function, all $\phi_i(\mathbf{x})$ must be smooth functions. To make the approximation of $f_i(\mathbf{x})$ more manageable, we define $\phi_i(\mathbf{x})$ to have only local support. The locations and the sizes of the supports depend on the nature of the problem and they are determined with the use of a self-organizing scheme.

The complete system using such a heterogeneous architecture is an assembly of modules m_i, each of which consists of one RBF unit and a small MLP. Each module m_i is assigned to approximate one of the component functions $f_i(\mathbf{x})$. The RBF unit in the module is used to define $\phi_i(\mathbf{x})$ and the MLP in the module is used to approximate $f(\mathbf{x})$ in the region where $\phi_i(\mathbf{x})$ is non-zero. The module output is the product of the RBF output and the MLP output. The output of the system is the sum of all the module outputs.

For a classification problem, one can introduce a threshold function in the output unit or one can provide binary classification output from every module. The latter approach can be used to provide fault-tolerance, if the domains of the ϕ_i overlap and the output unit performs some majority voting function.

As a feasibility study for one implementation of such a system, we have designed a circuit for implementing a RBF unit. In our design, a synaptic circuit generating a quadratic function consists of only two MOS transistors. The schematic diagram and the characteristics of the synaptic circuit are shown in figure 1.

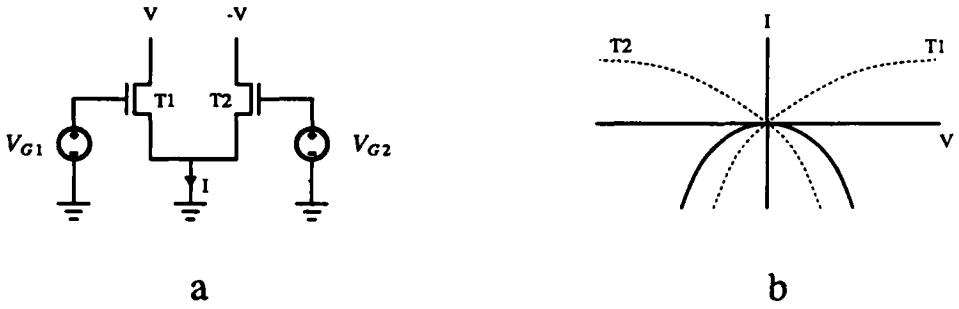

Figure 1 A Synaptic Unit of A Radial Basis Function Unit

The quadratic function (figure 1.b) can be adjusted by varying the bias voltages V_{G1} and V_{G2}. By replacing each MOS transistor with an EEPROM cell (Electrical Erasable Programmable Read Only Memory) which is specially developed for storing analog voltages, the bias voltages can then be stored in a non-volatile manner on the floating gate voltage of the EEPROM cell. Because of the compactness of this circuit, potentially hundreds of thousands of such circuits could be placed onto one VLSI chip.

We have produced the layout of such a synaptic circuit and submitted it to U.C. Berkeley's Microfabrication Facility. The wafers should be ready for testing in February.

Fault Tolerance in Artificial Neural Networks

Reed Clay (Professor C. H. Séquin)

We have examined different strategies for overcoming hardware failures in artificial neural networks. Our study focused on the failure of one or more units in the hidden layer of layered feed-forward networks. A failure is defined as a unit, the outputs of which remain stuck at a fixed value, regardless of its inputs. A typical basic failure is when a unit always outputs the middle value of its possible output range (i.e. an output voltage of 0 if the range is -1 to +1).

We investigated different types of retraining techniques to compensate for failures of hidden units in a network after it had learned a desired mapping. After a failure, the network was given additional training until it had again learned the desired mapping. We found that this technique was simple and effective provided that the network had more than the minimal number of units required to learn the mapping.

Subsequently, we found a practical technique to achieve true fault tolerance, i.e., to have the network continue to function correctly with NO additional training after failure of one or more hidden units. To achieve this fault-tolerant behavior, hidden units are randomly 'disabled' for some pattern presentations during a standard backpropagation training phase. We found that when the network was trained with 1, 2, or 3 hidden units disabled per pattern presentation, the network became robust to 1, 2, or 3 simultaneous failures of hidden units, respectively. The following results refer to the example of a decoder network that converts 21 points arranged in the shape of the standard seven-segment representation of the ten digits (with three points per segment) into the corresponding 10 domains. The network has 21 inputs, 14 hidden units, and 10 output units. The table below shows the number of trials required for the network to correctly classify the inputs with any combination of up to three hidden unit failures:

# of Fatalities	0	1	2	3
# of Trials	286	676	2066	15,118

This result holds for neutral failures (i.e. output clamped to the middle value of the possible range of output values) as well as for extreme-valued failures (i.e. output clamped to +1 for a unit with a possible range of -1 to +1), although somewhat longer training times are required in the latter case.

Furthermore, we found the surprising result that prolonged training in the single-fault mode can achieve fault tolerance even with respect to multi-fault patterns for which the network has not been trained specifically. This is shown in the table below. Here, the percentage of correctly learned mappings given single, double, and triple failures are listed after training the network for the number of trials shown but with only single failures during the training.

Trained with Single Fatality						
Number of trials	500	1000	5000	10,000	30,000	100,000
Test 1 fatality	94%	100%	100%	100%	100%	100%
Test 2 fatalities	62%	85%	99%	100%	100%	100%
Test 3 fatalities	30%	52%	82%	89%	95%	99%

This result also holds for extreme-valued failures, although additional training is required. The following table shows an example of this. Here, the hidden units that failed are set to the extreme value of +1, rather than the neutral value of 0 (output values in normal units range from -1 to +1).

Trained with Single Fatality						
Number of trials	500	1000	5000	10,000	30,000	100,000
Test 1 fatality	96%	99%	100%	100%	100%	100%
Test 2 fatalities	76%	84%	92%	93%	96%	98%
Test 3 fatalities	56%	66%	79%	81%	86%	90%

Our work so far has focused on networks that learn classifications tasks. Thus the network has to produce the desired outputs only within some threshold. Future investigations will look at networks that are trained to learn to approximate analog functions where the value of

the outputs must be as close as possible to the desired function value (i.e. not just thresholded to 0 or 1). Examining fault tolerance in this domain should give us a better quantitative understanding of how hidden unit failures can affect network behavior.

Neural Networks for Massively Parallel Computing
Arlindo Oliveira with Professor Alberto Sangiovanni-Vincentelli

Work on two main areas was begun in September. The first area is the study of a novel learning paradigm, based on the use of logic synthesis to perform rule induction from a specific set of examples. This approach, distinct from both the symbolic methods of classical AI and the connection approach which has been very favored lately, has potentialities not possessed by either of these latter two approaches.

Our approach was to implement a logic minimization algorithm, targeted for this particular application, and to test the idea with some examples, in order to evaluate its feasibility.

Preliminary results are encouraging, and point out further expansion of the algorithms developed. In all the examples tried, we succeeded in effectively deriving rules from specific examples, although the results are, in a few cases, worse than the ones obtained with other methods. Currently, work is in progress to perfect the developed algorithms, and to formalize the approach taken.

The second area concerns the efficient simulation of relevant biological systems. Specifically, we developed an efficient version of an electrical simulator targeted for the simulation of the hippocampus. Several techniques have been used to reduce the amount of computation involved in the detailed simulation of neural circuitry at the electrical level. In particular, non-linear relaxation and multirate simulation have been used to increase the simulator speed by a factor greater than 20 compared to the previous version that used sparse matrix techniques and the same time step for every circuit node.

This work is being developed in cooperation with Cornell Medical School and aims at simulating, using realistic models, a significant slice of the hippocampus region allowing us to study the short-to-long-term memory processes that are believed to take place in that region of the brain.

MPC.2. Systems Problems in Parallel Distributed Computation

Discrete Event Systems
Professor Pravin Varaiya

There is a growing need for new classes of models for systems constructed from interacting modules of discrete events, such as manufacturing systems, communication networks, and computer-controlled dynamical systems. Over the past two years we developed one class of such models called "Finitely recursive processes". It turns out that virtually all the ideas used in that model class can be extended to a large variety of such classes. More important, each class of models becomes a model "algebra", i.e. a set of models together with operators that combine models to form other models in ways in which real systems are interconnected. Thus the algebra provides ways for modelling systems as an interconnection of subsystems.

In [1] we present a general approach towards constructing such model algebras. The approach covers both deterministic and nondeterministic systems, and can be tailored to recover existing formalisms as well as to obtain new model families.

The control architecture of a continuous variable, continuous time plant is often divided into two layers. At the lower or servo layer is a controller that regulates the plant in the classical manner. At the upper layer the supervisor issues symbolic commands. Some time after a command is issued the supervisor receives a symbolic response indicating either that the command was executed or that an error condition occurred. The lower layer and the plant are modeled together by a set of differential equations. The supervisor, however, views the system as a whose behavior is described by a discrete event model such as a finite state machine. The two models must be related so that consistency is maintained. This question of consistency is posed and explored in [2].

Publications

[1] K. Inan and P. Varaiya, "Algebras of discrete event models" *Proc. IEEE* Vol 77(1), pp.24-38, January 1989.

[2] A. Gollu and P. Varaiya, "Hybrid dynamical systems" *Proc. 28th Conf. Decision and Control, pp. 2708-2712, Tampa, FL, December 1989.*

Dynamics of Neural Networks
Professor Eugene Wong with George Kesidis

Our principal findings during the reporting period concern the implementation of "Boltzmann Machines." The name notwithstanding, these are mathematical models of stochastic neural networks rather than machines. As models, Boltzmann Machines have played an important role in optimization and learning problems. We have discovered that these processes can indeed be realized in circuit form by suitably injecting noise into an analog or hybrid integrated circuit. So implemented, these will truly be machines, and a dramatic speedup of the computations associated with these models, such as simulated annealing, can be expected.

Publications

[1] E. Wong, "Implementing Boltzmann Machines," University of California Electronics Research Laboratory, *Tech. Memo. No. UCB/ERL M90/1*, January 1990.

Biological Motor Control -- Finger-Like Robot Systems
Professor Shankar Sastry with Karim Hollerbach

The progress reported here is part of an effort to characterize the dynamics of and possible control strategies for a biomechanical, multi-jointed finger, which is part of a class of systems which we call "finger-like robots." The following areas are of particular interest in this study:

- biomechanical muscle models to be integrated into the finger-like robot control scheme
- the dynamical behavior of finger-like robots
- The control of finger-like robots, as compared with that of "standard" robots as well as the control of biological multi-jointed muscle systems

Shown below is the abstract of a report about recent efforts in this area. The work described in the report provides a basis for future work with finger-like robot systems. By providing a simulation environment, the system described here allows the investigator to test various muscle models and control strategies and evaluate their performance.

> We have developed a simulator which improves upon the current software modules used to simulate finger-like robots. Our project is a window-based integrated dynamics simulator, which will include a new and more general model for robot dynamics. We currently use the Hill muscle model in our simulation to represent the finger-like robot actuators. With our simulator the user can easily vary the finger-like robot system parameters as well as simulate and view finger movement.
>
> Two modes of operation are possible. The user can specify a desired finger-like robot trajectory and a control law and observe the simulator as it attempts to follow the given trajectory for the finger-like robot. In the second mode of operation, the user specifies a file of actuator forces and then observes the resulting finger-like robot trajectory.
>
> The simulator has a modular design. As a result, it will be straightforward to implement future modifications and enhancements.

The report documents the design of the simulator. It also serves as a user's guide and a reference manual.

Hierarchical Control of Robotic Systems
Professor Shankar Sastry with Kristofer S.J. Pister

Robot control systems are increasingly required to control several manipulators working in concert. Given recent advances in both sensor and actuator technology, these manipulators themselves may present more difficult control problems. The computational aspect of this problem is clearly an area where parallel systems can have a dramatic impact. In order to make use of distributed computational resources, it was necessary to develop a paradigm by which hierarchical control of complex systems could be algorythmically broken down into a set of parallel tasks.

Inspired by the control system of the mammalian neuro-muscular system, we have developed a methodology for description of hierarchical control in a manner which is faithful to the underlying mechanics, structured enough to be used as an interpreted language, and sufficiently flexible to allow the description of a wide variety of systems. We have arrived at a consistent set of primitive operations which form the core of a robot system description and control language. This language is capable of describing a large class of robot systems under a variety of single level and distributed control schemes. Additionally, it provides a description of how processing and data flow is divided between multiple processing elements.

Publications

[1] D. Curtis Deno, Richard M. Murray, Kristofer S. J. Pister, Shankar Sastry. Primitives for Robot Control, *International Symposium on Mathematical Theory of Networks and Systems*, 1989

MPC.3. Interconnection of Dense Computational and Memory Elements

Analog Storage Devices for Neural Nets
Professors P. Ko and C. Hu with Alan Kramer, Victor Hu, Bhusan Gupta, Chi-Kai Sin, and Robert Chu

In 1989, we continued to investigate the suitability of EEPROM devices as reconfigurable analog storage elements for neural nets. In 1988, we developed a parallel programming feedback strategy using two fixed voltages to evaluate industrial EEPROM devices and achieved 8 bits(256 distinct values) of analog resolution. We also found the storage stability to be acceptable. These results were very encouraging and warranted further investigation[1].

However, further investigation of the EEPROM devices and construction of an experimental EEPROM-based neural network required detailed information about the device structures and the fabrication processes. Unfortunately, an industrial EEPROM silicon foundry was not available. Therefore, we decided to develop an in-house EEPROM technology. The first run of an NMOS EEPROM technology was completed in mid-1989 and functional devices were obtained. These devices were carried through testing procedures identical to those for the industrial devices. Similar results were obtained indicating that the in-house technology was functional.[2]

Subsequently, we carried out further testing on both the industrial and our own devices. One issue we investigated was how elevated temperature would affect a EEPROM device's storage stability and analog characteristics. We found that under normal operating conditions, instability of a stored state due to charge leakage was insignificant up to 150 °C, and the temperature behavior of the current-voltage characteristics of a EEPROM device was similar to that of a conventional MOSFET. We concluded from these findings that : (1)EEPROM-based neural nets are indeed feasible, and (2) conventional MOS VLSI circuit simulation CAD tools, after minor modifications, can be used to design EEPROM- based neural nets.[3]

At present, we are laying out a CMOS-EEPROM test chip. Test structures and circuits being implemented include a charge pump for on-chip high-voltage generation and a CCD(Charge-Coupled- Device) based injector for introducing constant charge packets into the EEPROM cell..

Publications

[1] V. Hu, A. Kramer, and P. Ko, "EEPROM as an Analog Storage Device for Neural Networks," *1st International Neural Network Society Meeting*, September 1988.

[2] A. Kramer, B. Gupta, and P. Ko, "EEPROM Based Analog Storage Device for Neural Net," presentation at the SnowBird Conference, April, 1989.

[3] A. Kramer, V. Hu, B. Gupta, C. K. Sin, R. Chu, and P. Ko "EEPROM Device as a Reconfigurable Analog Element for Neural Networks," *Technical Digest of the 1989 International Electron Device Meeting*, Washington D.C., Dec. 1989, p. 259.

Biologically-based Neural Studies
Professor E.R. Lewis with Bruce Parnas

The vertebrate auditory system provides an outstanding example of massively parallel signal processing. The cochlea creates a spectrographic image of the single-valued acoustic signal (sound pressure vs time) at each ear and transmits it to the brain over aprroximately 25,000 nerve fibers-- with various nerve fibers representing different regions of the spectrum. Human psycho-acoustic experiments clearly demonstrate that the brain analyzes the components of the monaural spectrograph for harmonic relationships, smoothness of spectral envelope, synchrony of onset, and commonality of modulation, and then segregates and integrates those components into subsets, each exhibiting spectral and temporal attributes (shared among its members) that are appropriate for an acoustic signal from a single physical source. Each integrated subset is labeled, often by the assignment of pitch, and is tracked over time as a single acoustic object. The human auditory system is highly tuned to the attributes expected from a single source; very slight mistuning of one or more components, slight asynchrony of onset, or slight lack of commonality of modulation allows the listener to segregate a subset further, into more than one

object. When spectrographs are available from both ears, the auditory system is able to refine its segregation by including binaural cues. The object of the research in this project is to reproduce in electronic hardware the acoutic segregation and integration capabilities of the brain.

To allow flexibility in the early phases of research on this project, we decided to use a flexible model of the cochlea, rather than a hard-wired version such as that of Lyon and Meade. Furthermore, convinced of the importance of neural-impulses for acoustic image processing (e.g., in detecting synchrony of spectrograph components), we decided to use realistic threshold models and realistic models of nerve-fiber signal conduction. We now have, in operation, a model that operates close to real time, with acoustic image processing over 10,000 independent nerve fibers from a 100-channel, highly flexible (programmable) cochlear model.

During the past twelve months, we made the following progress: (1) Serving as the beta test site for a state-of-the-art floating-point DSP board (Spectrum Signal Processing Board, DSP32C) that we identified as the most promising hardware for the cochlear model in our system, we identified and helped eliminate design flaws. (2) Subsequently, we incorporated two of these new boards into a very fast, dedicated PCAT clone that was intended to model the early stages of signal processing beyond the cochlea. (3) We developed software to implement cochlear models that can operate in real time with approximately 100 parallel filter channels and include the features we believe to be most important-- relatively broad band width, extremely steep high-frequency rolloff, and linear phase vs frequency relationship. By not restricting operation to real time, we can increase the number of filter channels almost without limit. (4) We developed software to implement a neural spike initiator model to translate the outputs of the cochlear filter channels into impulse trains; the model includes the features we believe to be most important-- all-or-none spike, refractoriness, realistic biasing and dithering with noise that is uncorrelated from one spike-initiator to the next. (5) We developed software

to translate the impulse patterns over a very large number of modeled nerve fibers into a visual display that can be interpreted easily by the investigator.

The software for the cochlear filter allows us to change the specifications of the individual channels quickly, and thus to test new configurations very easily. For our initial studies, we have installed a cochlear model filter model with 100 spectral channels spanning the frequency range from 125 Hz to 4000 Hz (more than adequate for most human psycho-acoustic tasks, including speech perception). Presently, each filter channel is expandied into 100 independently dithered spike-initiator models and 100 corresponding nerve-fiber models. Presently, to view the results of processing this image, we project it back to a 100-channel time-display, with each channel having a very wide dynamic range displayed logarithmically. Presently, our linear cochlear filter components are based on tuning curves from cat and gerbil cochleas (comparable human data being unobtainable), and incorporate relatively high dynamic order (graded from five at the low-frequency end to twenty-four at the high frequency end) and linear phase (for optimal preservation of temporal structure). Linear phase is approximated closely, but not achieved (of course) by the analog elements of the real cochlea.